U.S. Serial No. 09/729,010
Response to the Office Action of September 16, 2005

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-69. (Canceled)

70. (Currently amended) An apparatus for storing and retrieving digital video data, comprising:

an interface coupled to a system bus and configured to receive from the system bus a plurality of data bits arranged in a digital video data bit pattern;

a plurality of multiplexers, each configured to receive an associated one of the plurality of data bits in the digital video data bit pattern and its inverse, and configured to output one of the associated one of the plurality data bits or its inverse according to a preprogrammed bit altering scheme, the output of each of the plurality of multiplexers being combined to form an altered data bit pattern; and

a storage device coupled to the interface and configured to store the altered data bit pattern.

71. (Previously Presented) An apparatus as defined in claim 70, wherein the plurality of multiplexers are implemented in at least one of a hardware device, discrete logic device, or a software device.

72. (Previously Presented) An apparatus as defined in claim 71, wherein the hardware device is at least one of a field-programmable gate array, or an application specific integrated circuit.

73. (Previously Presented) An apparatus as defined in claim 70, wherein the preprogrammed bit altering scheme is based upon at least one of a serial number or a random number.

74. (Previously Presented) An apparatus as defined in claim 70, wherein the plurality of multiplexers are each further configured to receive, from the storage device, an associated one of the plurality of data bits in the altered data bit pattern and its inverse, and configured to select one of the data bits in the altered data bit pattern or its inverse according to the preprogrammed bit altering scheme, the output of each of the plurality of multiplexers being combined to restore the data bit pattern.

75. (Previously Presented) An apparatus as defined in claim 70, further comprising a second plurality of multiplexers, each configured to receive each of the data bits in the altered data bit pattern and to select a unique one of the data bits in the altered data bit pattern according to a preprogrammed bit scrambling scheme to output an altered and scrambled bit pattern, and

wherein the storage device is configured to store the altered and scrambled bit pattern.

76. (Currently amended) An apparatus for storing and retrieving digital video data, comprising:

an interface coupled to a system bus and configured to receive from the system bus a plurality of data bits arranged in a data bit pattern;

a plurality of multiplexers, each configured to receive each of the plurality of data bits in the data bit pattern and to select a unique one of the data bits according to a preprogrammed bit scrambling scheme, the output of each of the plurality of multiplexers being combined to form a scrambled data bit pattern; ~~and~~

a second plurality of multiplexers, each configured to receive an associated one of the plurality of data bits in the scrambled data bit pattern and its inverse, and configured to output one of the associated one of the plurality of data bits or its inverse according to a preprogrammed bit altering scheme, the output of each of the second plurality of multiplexers being combined to form a scrambled and altered data bit pattern, and

a storage device coupled to the interface and configured to store the scrambled and altered data bit pattern.

77. (Currently amended) An apparatus as defined in claim 76, wherein the plurality of multiplexers and the second plurality of multiplexers are implemented in at least one of a hardware device, discrete logic device, or a software device.

78. (Previously Presented) An apparatus as defined in claim 77, wherein the hardware device is at least one of a field-programmable gate array, or an application specific integrated circuit.

79. (Previously Presented) An apparatus as defined in claim 76, wherein the preprogrammed bit scrambling scheme is based upon at least one of a serial number or a random number.

80. (Currently amended) An apparatus as defined in claim 76, wherein the second plurality of multiplexers are each further configured to receive, from the storage device, an associated one of the plurality of data bits in the scrambled and altered data bit pattern and its inverse, and configured to select one of the data bits in the scrambled and altered data bit pattern or its inverse according to the preprogrammed bit altering scheme, the output of each of the second plurality of multiplexers being combined to restore the scrambled data bit pattern, and wherein the plurality of multiplexers are each further configured to receive each of the plurality of data bits in the scrambled data bit pattern and to select a unique one of the data bits according to the preprogrammed bit scrambling scheme, the output of each of the plurality of multiplexers being combined to restore the data bit pattern.

81. (Canceled)

82. (Previously Presented) A method for storing and retrieving digital data within a storage device, the method comprising:

receiving data bits across a bus, the data bits forming a bit pattern;

inputting into at least one multiplexer, an associated one of the data bits and its inverse for each of the data bits forming the bit pattern;

altering the bit pattern of the data bits to form an altered bit pattern by selecting one of the associated one of the data bits or its inverse for each of the data bits forming the bit pattern based upon a preprogrammed data altering scheme to form the altered bit pattern;

storing the altered bit pattern;

restoring the altered bit pattern to the bit pattern by inputting into the multiplexer, an associated one of the altered data bits and its inverse for each of data bits in the altered bit pattern, and selecting one of the associated one of the altered data bits or its inverse based upon the preprogrammed data altering scheme; and

outputting the restored data bits.

83. (Previously Presented) A method according to claim 82, wherein the altering and the restoring are performed by one of a discrete logic device, a software device, a field-programmable gate array, or an application specific integrated circuit.

84. (Previously Presented) A method according to claim 82, wherein the altering and the restoring are unique to the storage device.

85. (Previously Presented) A method according to claim 82, wherein the preprogrammed data altering scheme is based upon at least one of a serial number or a random number generator.

86. (Previously Presented) A method according to claim 82, further comprising:

scrambling the altered data bits prior to storing to form an altered and scrambled bit pattern by inputting into at least one second multiplexer each of the data bits forming the altered bit pattern and selecting a unique one of the altered data bits according to a preprogrammed bit scrambling scheme to form an altered and scrambled bit pattern;

storing the altered and scrambled bit pattern; and

restoring the altered and scrambled bit pattern to the altered bit pattern by inputting into the at least one second multiplexer each of the altered and scrambled data bits and selecting a unique one of the altered and scrambled data bits according to the preprogrammed bit scrambling scheme to form the altered bit pattern.

87. (Currently amended) A method for storing and retrieving digital data within a storage device, the method comprising:

receiving data bits across a bus, the data bits forming a bit pattern;

inputting into at least one multiplexer, each of the data bits forming the bit pattern;

scrambling the bit pattern to form a scrambled bit pattern by selecting a unique one of the data bits in each of the at least one multiplexer based upon a preprogrammed data scrambling scheme to form the scrambled bit pattern;

altering the scrambled data bit pattern to form a scrambled and altered bit pattern by inputting each of the data bits of the scrambled bit pattern and its inverse into an associated one of at least one second multiplexer and selecting one of the data bits or its inverse based upon a preprogrammed data altering scheme to form a scrambled and altered data bit pattern;

storing the scrambled and altered data bit pattern;

restoring the scrambled and altered data bit pattern to the scrambled bit pattern by inputting into the at least one second multiplexer an associated one of the data bits of the altered and scrambled data pattern and its inverse, and selecting data bits of the altered and scrambled data pattern or its inverse according to the preprogrammed bit altering scheme to form the scrambled bit pattern.;

restoring the scrambled bit pattern to the bit pattern by inputting into the at least one multiplexer, each of the data bits of the scrambled bit pattern, and selecting a unique one of the data bits of the scrambled bit pattern based upon the preprogrammed data scrambling scheme; and

outputting the restored data bits.

88. (Currently amended) A method according to claim 87, wherein the scrambling, the altering, and the restoring are performed by one of a discrete logic device, a software device, a field-programmable gate array, or an application specific integrated circuit.

89. (Currently amended) A method according to claim 87, wherein the scrambling, the altering, and the restoring are unique to the hardware platform

90. (Previously Presented) A method according to claim 87, wherein the preprogrammed data scrambling scheme is based upon at least one of a serial number or a random number generator.

91. (Canceled)